UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,130	02/06/2004	Qadeer A. Khan	SC13024IC	8393

23125 7590 03/03/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,130	KHAN ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *10-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

A. Figures 1 and 3 (claims 1-9).

B. Figures 5 and 6 (claims 10-15).

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there is no generic claim.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the

examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

2. During a telephone conversation with Mr. Robert King on 3/1/05 a provisional election was made with traverse to prosecute the invention of specie A (Figures 1 and 3, claims 1-9). Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-15 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

3. The drawings are objected to because Figure 3 of the drawings fails to label --Vss-- at the sources of NMOS transistors 308 and 312 (see specification, paragraphs [0036] and [0038]). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1-9 are objected to because of the following informalities:

Claim 1, line 2, "shifting a" should be changed to --shifting the--.

Claim 1, line 3, "to a low" should be changed to --to the low--.

Claim 1, line 16-17, it appears that "as an input" should be changed to --as the input-- to avoid unclear antecedent basis since "an input" was recited earlier in the claim (see line 7).

Claim 1, line 20, it appears that "as an output" should be changed to --as the output-- to avoid unclear antecedent basis since "an output" was recited earlier in the claim (see line 11).

Claims 2-5 are objected to because they include the minor informalities of claim 1.

Claim 6, line 15-16, it appears that "as an input" should be changed to --as the input-- for the similar reason as discussed in claim 1.

Claim 6, line 19, it appears that "as an output" should be changed to --as the output— for the similar reason as discussed in claim 1.

Claims 7-8 are objected to because they include the minor informalities of claim 6.

Claim 9, line 15-16, it appears that "as an input" should be changed to --as the input-- for the similar reason as discussed in claim 1.

Claim 9, line 19, it appears that "as an output" should be changed to --as the output— for the similar reason as discussed in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ng et al. (USP 5,877,633).

With respect to claim 1, Figures 1-2 of the Ng et al. reference discloses a bidirectional level shifter (102, wherein the detail of 102 is shown in Figure 2) for shifting a low voltage digital signal (106, see lines 2-6 of Col. 2) to a high voltage signal (108, see lines 2-6 of Col. 2), and for shifting the high voltage digital signal (108) to the low voltage digital signal (106), wherein Figure 2 shows the bidirectional level shifter (102) comprises: a first I/O terminal (200) for sending and receiving the low voltage digital signal (106); a second I/O terminal (202) for sending and receiving the high voltage digital signal (108); a first circuit (213) coupled to the first and second I/O terminals (200 and 202) wherein the first circuit (213) operates at a low power supply voltage (because circuit 213 is used for shifting a high voltage signal 202 into a low voltage signal 200, so circuit 213 must operates at the low power supply voltage); and a second circuit (212) coupled to the first and second I/O terminals (200 and 202) wherein the first circuit (212) operates at a high power supply voltage (because circuit 212 is used for shifting a low voltage signal 200 into a high voltage signal 202, so circuit 212 must operates at the high power supply voltage).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ng et al. (USP 5,877,633) in view of Nguyen et al. (USP 6,842,043).

With respect to claims 2-4, the circuit in Figure 2 of the Ng et al. reference discloses a bidirectional level shifter which meets all of the limitations of the claim except that the detail of each of the first and second circuits comprising two PMOS transistors, two NMOS transistors and an inverter connected as recited in claims 2 and 4. However, Figure 3 of the Nguyen et al. reference discloses a unidirectional shifter that has an advantage of faster switching and thus the speed of the circuitry is faster (see lines 30-35 of Col. 8 of Nguyen et al.). Therefore, it would have been obvious to one having skills in the art at the time the inventions was made to modify the bidirectional level shifter circuit in Figure 2 of the Ng et al. reference by specifically using the unidirectional level shifter (Figure 3 of Nguyen et al.) for each of the first (213) and second (212) circuits in Figure 2 of the Ng et al. reference for the purpose of improving the speed of the circuitry. Thus, this combination/modification meets all the limitations of claims 2 and 4. Note that, in claims 2-3, the first circuit (i.e., Figure 3 of Nguyen et al. which replaces circuit block 213 in Figure 2 of Ng et al.) comprising: a first PMOS transistor (P1), a second PMOS transistor (P2), a first NMOS (N1), a second NMOS (N2), a first inverter (P3, N3), a fifth PMOS transistor (P5), a fifth NMOS

transistor (N5), output (OUT) in Figure 3 of Nguyen et al. is connected to node 200 in Figure 2 of Ng et al. (because output of first circuit 213 connected to node 200 in Figure 2 of Ng et al.), input (IN) in Figure 3 of Nguyen et al. is connected to node 202 in Figure 2 of the Ng et al. (because input of the first circuit 213 is connected to 202 in Figure 2 of Ng et al.), reference voltage (ground), and power supply voltage (Hi-V) in Figure 3 of Nguyen et al. in this case is changed to be the low supply voltage Lo-V since the circuit 213 must be operated by the low voltage to shift the signal from the high voltage into the low voltage, and voltage (Lo-V) for inverter (P3, N3) must be changed to Hi-V since the input of the first circuit 213 receives the signal at a high voltage level to shift into the low voltage level at the output of 213. Note that in claims 4-5, the second circuit (i.e., Figure 3 of Barnes which replaces circuit block 212 in Figure 2 of Ng et al.) comprising: a third PMOS transistor (P1), a fourth PMOS transistor (P2), a third NMOS (N1), a fourth NMOS (N2), a second inverter (P3, N3), a sixth PMOS transistor (P5) and a sixth NMOS transistor (N5), output (OUT) in Figure 3 of Nguyen et al. is connected to node 202 in Figure 2 of Ng et al. (because output of first circuit 212 connected to node 202 in Figure 2 of Ng et al.), input (IN) in Figure 3 of Nguyen et al. is connected to node 200 in Figure 2 of the Ng et al. (because input of the first circuit 212 is connected to 200 in Figure 2 of Ng et al.), reference voltage (ground) and power supply voltage (Hi-V in Figure 3 of Nguyen et al. in this case is the high supply voltage since the circuit 212 must be operated by the high voltage to shift the signal from the low voltage into the high voltage).

Claims 6-9 are rejected for the same manner as discussed in the above combination/modification with regard to the rejection of claims 4-6.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 2, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816